Text VRAM

Memory block 38h

<table>
<tr><th>offset</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>0000h
:
07FFh</td><td>R / W</td><td>Text 1
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>function</th><td colspan="8">A [10: 3]</td></tr>
</table>
A [10: 3] is valid for PCG that specifies the Kanji ROM address A [16: 3] together with text 1/2.
A [3] (Bit0) is ignored in 1-character 16-line mode.</td></tr>
<tr><td>0800h
:
0FFFh</td><td>R / W</td><td>attribute
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>function</th><td>BL</td><td>RV</td><td colspan="2">S [1: 0]</td><td>P</td><td>G</td><td>R</td><td>B</td></tr>
</table>
<table>
<tr><td>BL</td><td>Blink</td><td>0: Blink disabled
1: Blink enabled</td></tr>
<tr><td>RV</td><td>reverse</td><td>0: Reverse disabled
1: Reverse enabled</td></tr>
<tr><td>S</td><td>Single color PCG selection</td><td>00: PCG0
01: PCG1
10: PCG2
11: PCG3</td></tr>
<tr><td>P</td><td>8 color PCG selection</td><td>0: Kanji ROM / single color PCG
1: 8 color PCG</td></tr>
<tr><td>GRB</td><td>Letter color</td><td>Kanji ROM / single color PCG character color
<table>
<tr><th>GRB</th><th>color</th><th>GRB</th><th>color</th></tr>
<tr><td>000</td><td>■ Black</td><td>100</td><td>■ Green</td></tr>
<tr><td>001</td><td>■ Blue</td><td>101</td><td>■ Cyan</td></tr>
<tr><td>010</td><td>■ Red</td><td>110</td><td>■ Yellow</td></tr>
<tr><td>011</td><td>■ Magenta</td><td>111</td><td>□ White</td></tr>
</table></td></tr>
</table>
<table>
<tr><th>P</th><th>S</th><th>K</th><th>mode</th></tr>
<tr><td>0</td><td>00</td><td>1</td><td>Kanji ROM</td></tr>
<tr><td>0</td><td>00</td><td>0</td><td>PCG0 (single color)</td></tr>
<tr><td>0</td><td>01 01</td><td>---</td><td>PCG1 (single color)</td></tr>
<tr><td>0</td><td>Ten</td><td>---</td><td>PCG2 (single color)</td></tr>
<tr><td>0</td><td>11</td><td>---</td><td>PCG3 (single color)</td></tr>
<tr><td>1</td><td>---</td><td>---</td><td>Superposition of PCG1 / 2/3 (8 colors)</td></tr>
</table>
* Kanji / single color PCG is treated as transparent where there are no dots, but in the case of 8-color PCG, black is treated as transparent.
* Attributes are processed in the order of blink → reverse → color specification.</td></tr>
<tr><td>1000H
:
17FFh</td><td>R / W</td><td>Text 2
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>function</th><td>K</td><td>L</td><td colspan="6">A [16:11]</td></tr>
</table>
<table>
<tr><td>K</td><td>Kanji / PCG</td><td>0: PCG
1: Kanji ROM</td></tr>
<tr><td>L</td><td>Level 1 / Level 2 Kanji selection</td><td>0: Level 1 Kanji
1: Level 2 Kanji</td></tr>
</table></td></tr>
</table>

Kanji ROM address

Character type	address	Value to write in VRAM
Non-kanji	0000h ~	8000h + ((JIS_H -21h) * 60h + (JIS_L -20h)) * 4
Level 1 Kanji	8000h ~	9000h + ((JIS_H -30h) * 60h + (JIS_L -20h)) * 4
Level 2 Kanji	20000h ~	C000h + ((JIS_H -50h) * 60h + (JIS_L -20h)) * 4
ANK (16 lines)	6000h ~	8C00h + (ASCII * 4)
ANK (8 lines)	6010h ~	8C02h + (ASCII * 4)
MZ-2000 CGROM	6018h ~	8C03h + (ASCII * 4)
MZ-700 CGROM (equivalent to 0000h-03FFh)	4400h ~	8880h + DISPCODE
MZ-700 CGROM (equivalent to 0C00h-0FFFh)	5C00h ~	8B80h + (DISPCODE -80h)

* MZ-700 CGROM display codes 66h (&) and 67h (') are replaced with double diagonal line patterns. There is no MZ-700 katakana / lowercase letter pattern.

PCG RAM

Memory block 39h

offset	R / W	Explanation
0000h : 07FFh	R / W	PCG0 or Kanji ROM (specified by port CFh)
0800h : 0FFFh	R / W	PCG1
1000H : 17FFh	R / W	PCG2
1800h : 1FFFh	R / W	PCG3

As for the bitmap pattern of PCG RAM / Kanji ROM, MSB (Bit7) is on the left side and LSB (Bit0) is on the right side. Note that it is the opposite of GVRAM.

RS-232C / mouse

address	R / W	Explanation
A0h	R / W	Z80SIO channel A data
A1h	R / W	Z80SIO Channel A Control
A2h	R / W	Z80SIO channel B data
A3h	R / W	Z80SIO Channel B Control

* Address can be changed to B0h-B3h with Bit7 of I / O CDh
Channel B function (RS-232C / mouse) can be selected with IOA [3] of OPN

Memory mapping register

address	R / W	Explanation

B4h W

Bit	7	6	Five	Four	3	2	1	0
signal						MRSEL		

Select the memory mapping register
to be read / written by B5h After reading / writing B5h, the value of B4h is auto-incremented.

MRSEL	Memory address	MRSEL	Memory address
0	0000h-1FFFh	Four	8000h-9FFFh
1	2000h-3FFFh	Five	A000h-BFFFh
2	4000h-5FFFh	6	C000h-DFFFh
3	6000h-7FFFh	7	E000h-FFFFh

B5h R / W

Bit	7	6	Five	Four	3	2	1	0
signal		MB						

Memory block number to allocate

MB	Memory block	Weight at the time of access
00h-0Fh	Main RAM (8Kx16 = 128K)	+1 during M1 cycle
10h-1Fh	Extended RAM (8Kx16 = 128K)	+1 during M1 cycle
20h-27h	Standard graphic VRAM (B / R / G / I)	+1 (*)
28h-2Fh	Extended graphics VRAM (B / R / G / I)	+1 (*)
30h-31h	Standard Graphic VRAM (Read-Modify-Write)	+2 (*)
32h-33h	Extended Graphic VRAM (Read-Modify-Write)	+2 (*)
34h-37h	IPL ROM	+1 during M1 cycle
38h	Text VRAM	+1 (*)
39h	Kanji ROM / PCG	+2 (*)
3Ah	Dictionary ROM	???
3Ch-3Fh	Communication ROM	+1 during M1 cycle

(*) M1 cycle is not possible ・ If you access during the display period, a separate weight will be charged until the blanking period

According to a survey by X1 Center , the CPU accessible period of graphic VRAM is
24KHz: memory write cycle + 50 clocks + memory write cycle
15KHz: memory write cycle + 91 clocks + memory write cycle
Normal access read-modify write with additional weight +1, +2 respectively, but the above values do not change

Graphic controller

BCh W

Bit	7	6	Five	Four	3	2	1	0
signal	INC	0	0	REGNO				

If
auto-increment is specified to select the register to be written by BDh, **only** the **lower 2 bits** of REGNO are incremented by 1 after writing the value to BDh.

REGNO	Graphic controller register number	00h-18h
INC	Auto increment after BDh writing	0: Invalid 1: Valid

BCh R

Direct read, B screen read data
Select read, select read data

BDh W

Write port to the graphics controller register specified in BCh

	R	At the time of direct read, at the time of R screen read data select read **Bit** 7 6 Five Four 3 2 1 0 **signal** $\overline{\text{VBLANK}}$ CLR **$\overline{\text{VBLANK}}$** Vertical blanking signal: 0: Vertical blanking period 1: Vertical display period **CLR** Screen clear end bit: 0: End 1: Running
BEh	R	Direct read, G screen read Data select read, indefinite
BFh	R	Direct read, I screen read Data select read, indefinite

Graphic controller internal register

register	Explanation
00h	Pattern register B
01h	Pattern register R
02h	Pattern register G
03h	Pattern register I
04h	Color register **Bit** 7 6 Five Four 3 2 1 0 **signal** I G R B
05h	Function register / screen selection register **Bit** 7 6 Five Four 3 2 1 0 **signal** FN I G R B **FN** function: 00: REPLACE 01: PSET 10: Clear screen **I / G / R / B** Drawing plane selection: 0: Do not draw 1: Draw **REPLACE** Only the plane specified in the screen selection register (05h) is to be rewritten . For each specified plane, 1. AND the VRAM data with the inverted value of the bitmask register 2. OR (CPU write data AND pattern register AND bit mask register value) only for the plane specified by the color register (04h). 3. Write the result to VRAM (Image of making a hole in VRAM with the bit mask register value and fitting the pattern cut out with the CPU write value) **PSET** Only the plane specified in the screen selection register (05h) is to be rewritten . For each specified plane, 1. AND the VRAM data with the inverted value of CPU write data 2. OR (CPU write data AND pattern register) only for the plane specified by the color register (04h). 3. Write the result to VRAM (Image of making a hole in VRAM with the CPU write value and fitting the pattern exactly there)

06h

Bit mask register

07h

Select read control register

Bit	7	6	Five	Four	3	2	1	0
signal				0			A	
				1	I	G	R	B

A	Direct read read plane	00: B 01: R 10: G 11: I
I / G / R / B	Select lead specified color	

08h, 09h

Display area Vertical start line setting

Port	09h								08h							
Bit	7	6	Five	Four	3	2	1	0	7	6	Five	Four	3	2	1	0
signal									GDEVS							

Specify the number of rasters with 9 bits
0 to 190h (for vertical 400 lines)
0 to C8h (for vertical 200 lines)

0Ah, 0Bh

Display area vertical end line setting

Port	0Bh								0Ah							
Bit	7	6	Five	Four	3	2	1	0	7	6	Five	Four	3	2	1	0
signal									GDEVE							

Similar to GDEVS

0Ch

Display area Horizontal start setting

Bit	7	6	Five	Four	3	2	1	0
signal		GDEHS						

0 to 50h
Horizontal 640 dots, 8 dot units
Horizontal 320 dots, 4 dot units

0Dh

Display area horizontal stop setting

Bit	7	6	Five	Four	3	2	1	0
signal		GDEHE						

Similar to GDEHS

0Eh

Display mode switching

Bit	7	6	Five	Four	3	2	1	0
signal	EX	0	0	$\overline{4C}$	256C	V200	H640	PRI

EX	Standard VRAM / Extended VRAM selection	0: Standard VRAM 1: Extended VRAM
$\overline{4C}$	4-color mode (only in 640x400 mode)	0: 4-color mode 1: 16-color or 256-color mode
256C	256 color (8 plane simultaneous output) mode	0: 16 color mode 1: 256 color mode
V200	Number of vertical lines	0: 400 line 1: 200 line
H640	Number of horizontal dots	0: 320 dots 1: 640 dots
PRI	Priority when superimposing two screens (320x200 16-color mode only, specify 1 in other modes)	0: The screen with the younger number is in the back 1: The screen with the younger number is in the foreground

When EX is set to 1, the behavior is such that GCRTC always ORs 4000h to the address when accessing GVRAM for screen display. By using the scroll register in the range of 0000h-3FFFh, it is possible to switch

the standard VRAM / extended VRAM page with only this bit without changing the scroll register setting. However, it is just that function, so if you treat the standard VRAM / extended VRAM as a linear space of 0000h-7FFFh, you can leave it at 0. EX is ignored in 640x400 mode

0Fh

Horizontal dot scroll amount in the scroll area

Bit	7	6	Five	Four	3	2	1	0
signal						HSCRL		

Side-scrolling amount 0 to 7 in 1-dot units The
specified number of white pixels are inserted from the left edge of the screen, and the screen shifts to the right (scrolls) by that amount,
so it is necessary to remove the left edge from the display area and hide it
320x200 2 screen mode And in 256 color mode, this function can be used only on screens 0 and 2, so smooth scrolling is virtually impossible.

10h, 11h

Upper left address of the screen

Port	11h								10h							
Bit	7	6	Five	Four	3	2	1	0	7	6	Five	Four	3	2	1	0
signal		SAD0														

12h, 13h

Scroll wrap address

Port	13h								12h							
Bit	7	6	Five	Four	3	2	1	0	7	6	Five	Four	3	2	1	0
signal		SAD1														

When the CRTC VRAM read address counter reaches this address, the address counter returns to 0000h from the next read.

14h, 15h

Display address after scrolling end line

Port	15h								14h							
Bit	7	6	Five	Four	3	2	1	0	7	6	Five	Four	3	2	1	0
signal		SAD2														

When the display raster reaches the
scroll end line, it is not affected by horizontal dot scrolling (HSCRL, 0Fh) after the scroll end line that starts displaying from this address.

16h, 17h

Scroll end line

Port	17h								16h							
Bit	7	6	Five	Four	3	2	1	0	7	6	Five	Four	3	2	1	0
signal									SL1							

0 to 190h (when vertical 400 lines)
0 to C8h (when vertical 200 lines)

18h

Screen display register

Bit	7	6	Five	Four	3	2	1	0
signal	I1	G1	R1	B1	I0	G0	R0	B0

A plane with bit 1 is displayed

Interrupt control (I / O controller)

address	R / W	Explanation
C6h	W	Control of interrupts ($\overline{\text{VBLANK}}$, 8253, printer, RTC) handled by the I / O controller

Bit	7	6	Five	Four	3	2	1	0
signal	VSEN				VBLKIE	TMIE	PRTIE	RTCIE

VSEN	The interrupt vector set command C7h must not have more than one bit to select the interrupt vector setting target.	1000: Set interrupt vector for $\overline{\text{VBLANK}}$ interrupt 0100: Set interrupt vector for timer (8253) interrupt

				0010: Set interrupt vector for printer interrupt 0001: Set interrupt vector for RTC interrupt
		VBLKIE	$\overline{\text{VBLANK}}$ interrupt enabled	0: Interrupt disabled 1: Interrupt enabled
		TMIE	Timer (8253) interrupt enabled	0: Interrupt disabled 1: Interrupt enabled
		PRTIE	Printer interrupt enabled	0: Interrupt disabled 1: Interrupt enabled
		RTCIE	RTC interrupt enabled	0: Interrupt disabled 1: Interrupt enabled
		Note that the source of the $\overline{\text{VBLANK}}$ interrupt is the VBLANK signal from the graphics controller.		
C7h	W	Interrupt vector write port		

OPN

ϕM =
1 weight is added when accessing 2MHz

address	R / W	Explanation
C8h	W	Register number
	R	status **Bit** 7 6 Five Four 3 2 1 0 **signal** BUSY TFLGB TFLGA **BUSY** Command / data interface BUSY flag — 0: Ready 1: Busy **TFLGB** Timer-B end flag — 0: Counting 1: Counting end **TFLGA** Timer-A end flag — 0: Counting 1: Counting end
C9h	R / W	Register access

OPN GPIO

SSG register	R / W	Explanation
07h	W	I / O settings for I / O ports A and B **Bit** 7 6 Five Four 3 2 1 0 **signal** IOB IOA noise tone **IOB** I / O port B input / output — 0: Input 1: Output **IOA** I / O port A input / output — 0: Input 1: Output On the MZ-2500, set port A as output and port B as input.
0Eh	W	I / O port A **Bit** 7 6 Five Four 3 2 1 0 **signal** VACL VOE VBUSY VDATA MOUSE $\overline{\text{PLT}}$ DRSEL READYA **VACL** Voice board reset bit — 0: Normal operation 1: Reset voice board **VOE** Voice board ROM designation — 0: Internal ROM

				1: External ROM
		VBUSY	Voice board handshake bit	
		VDATA	Voice board transmission data	
		MOUSE	SIO B channel function selection	0: RS-232C (9 pin) 1: Mouse
		$\overline{\text{PLT}}$	4096 color palette board output selection	0: Select 4096 color palette board output 1: Select main unit output
		DRSEL	Swap FDD drive numbers	0: Built-in FDD 0,1 / External FDD 2,3 1: External FDD 0,1 / Built-in FDD 2,3
		READYA	RS-232C RR signal (D-Sub 25-pin connector pin 11)	

0Fh — R

I / O port B

Bit	7	6	Five	Four	3	2	1	0
signal	VACK	$\overline{\text{RASTER}}$	$\overline{\text{80B}}$	$\overline{\text{2000}}$	$\overline{\text{ALARM}}$	CDB	CIA	CDA

VACK	Acnoridge from voice board	
$\overline{\text{RASTER}}$	Display output mode	0: 400 line (24kHz) 1: 200 line (15kHz)
$\overline{\text{80B}}$	MZ-80B mode	0: 80B mode
$\overline{\text{2000}}$	MZ-2000 mode	0: 2000 mode
$\overline{\text{ALARM}}$	RTC ALARM output	
CDB	RS-232C CD signal (D-Sub 9-pin connector, pin 9)	
CIA	RS-232C CI signal (D-Sub 25-pin connector, pin 22)	
CDA	RS-232C CD signal (D-Sub 25-pin connector pin 8)	

Telephone control port

CAh

R

Bit	7	6	Five	Four	3	2	1	0
signal	POWER		$\overline{\text{CONEC}}$	$\overline{\text{CMSTB}}$	$\overline{\text{CMD3}}$	$\overline{\text{CMD2}}$	$\overline{\text{CMD1}}$	$\overline{\text{CMD0}}$

POWER	1: Powered on from the phone
$\overline{\text{CONEC}}$	0: Voice line is connected
$\overline{\text{CMSTB}}$	0: $\overline{\text{CM [3: 0]}}$ valid
$\overline{\text{CMD [3: 0]}}$	Data from the phone unit

W

Bit	7	6	Five	Four	3	2	1	0
signal				TOFF				

TOFF	Power off with 0 → 1 → 0

RTC RP5C15

16-bit I / O access
3 waits are added when accessing

address	R / W	Explanation
CCh	R / W	CPU address [11: 8] is connected to A [3: 0] on RP5C15

SIO baud rate selection (I / O controller)

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>CDh</td><td>W</td><td>
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>signal</th><td>A</td><td></td><td colspan="2">TxRxCA</td><td colspan="4">TxRxCB</td></tr>
</table>
<table>
<tr><td>A</td><td>SIO I / O address selection</td><td>0: A0h-A3h
1: B0h-B3h</td></tr>
<tr><td>TxRxCA</td><td>SIO Channel A Baud Rate</td><td rowspan="2">
<table>
<tr><th>TxRxC</th><th>Output pin frequency</th><th>Baud rate (SIO x16 mode)</th></tr>
<tr><td>000</td><td>307kHz</td><td>19200</td></tr>
<tr><td>001</td><td>154kHz</td><td>9600</td></tr>
<tr><td>010</td><td>76.9kHz</td><td>4800</td></tr>
<tr><td>011</td><td>38.4kHz</td><td>2400</td></tr>
<tr><td>100</td><td>19.2kHz</td><td>1200</td></tr>
<tr><td>101</td><td>9600Hz</td><td>600</td></tr>
<tr><td>110</td><td>4800Hz</td><td>300</td></tr>
<tr><td>111</td><td>2400Hz</td><td>150</td></tr>
</table>
</td></tr>
<tr><td>TxRxCB</td><td>SIO channel B baud rate</td></tr>
</table>
</td></tr>
</table>

Dictionary ROM bank switching

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>CEh</td><td>W</td><td>
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>signal</th><td colspan="3"></td><td colspan="5">BANK</td></tr>
</table>
<table>
<tr><td>BANK</td><td>Bank switching of dictionary ROM (memory block 3Ah)</td><td>00h-1Fh</td></tr>
</table>
</td></tr>
</table>

PCG / Kanji ROM bank switching

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>CFh</td><td>W</td><td>
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>signal</th><td>K</td><td colspan="7">BANK</td></tr>
</table>
<table>
<tr><td>K</td><td>PCG / Kanji ROM (memory block 39h) switching</td><td>0: PCG
1: Kanji ROM</td></tr>
<tr><td>BANK</td><td>Bank switching of Kanji ROM (memory block 39h)</td><td>00h-7Fh</td></tr>
</table>
</td></tr>
</table>

FDD I / F (MB8876)

1 weight is added at the time of access

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td rowspan="2">D8h</td><td>R</td><td>Status register</td></tr>
<tr><td>W</td><td>Command register</td></tr>
<tr><td>D9h</td><td>R / W</td><td>Track register</td></tr>
<tr><td>DAh</td><td>R / W</td><td>Sector register</td></tr>
<tr><td>DBh</td><td>R / W</td><td>Data register</td></tr>
<tr><td>DCh</td><td>W</td><td>Motor / drive select control register
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>signal</th><td>M-ON</td><td colspan="3"></td><td>DSEN</td><td colspan="2">DS</td></tr>
</table>
</td></tr>
</table>

		M-ON FDD motor control: 0: OFF 1: ON **DSEN** Drive select enabled: 0: Drive select disabled 1: Select the drive with the number specified by DS **DS** Drive select: Drive number to select
DDh	W	Head select control register **Bit** 7 6 Five Four 3 2 1 0 **signal** HS **HS** Head select: 0: Side 0 1: Side 1
DEh	W	Single density / double density control register **Bit** 7 6 Five Four 3 2 1 0 **signal** FM **FM** Single density / double density selection: 0: Double density (MFM) 1: Single density (FM)

8255 PPI

address	R / W	Explanation
E0h	W	8255 Port A cassette control **Bit** 7 6 Five Four 3 2 1 0 **signal** $\overline{\text{APSS-P}}$ $\overline{\text{APLAY}}$ $\overline{\text{AREW}}$ VID $\overline{\text{STOP}}$ $\overline{\text{PLAY}}$ $\overline{\text{FF}}$ $\overline{\text{REW}}$ * Only the functions of MZ-2500 / 2000 mode are described. **$\overline{\text{APSS-P}}$** APSS operation during fast forward / rewind: 0: Do APSS 1: Do not APSS **$\overline{\text{APLAY}}$** Operation at the end of rewinding: 0: Play 1: Stop **$\overline{\text{AREW}}$** Operation at tape end: 0: Rewind 1: Stop **VID** Monochrome screen inversion: 0: Invert 1: Do not invert **$\overline{\text{STOP}}$** Stop: Stop at 1 → 0 → 1 **$\overline{\text{PLAY}}$** Playback / recording: Play / record from 1 → 0 → 1 **$\overline{\text{FF}}$** Fast forward: Fast forward with 1 → 0 → 1 **$\overline{\text{REW}}$** Rewind: Rewind by 1 → 0 → 1
E1h	R	8255 Port B cassette control **Bit** 7 6 Five Four 3 2 1 0 **signal** PB7 READ $\overline{\text{TREADY}}$ $\overline{\text{WREADY}}$ TEND $\overline{\text{VBLANK}}$ **PB7** Z80B PIO PB7 **READ** Data read from the data recorder **$\overline{\text{TREADY}}$** 0: Tape is set in the data recorder 1: Tape is not set in the data recorder **$\overline{\text{WREADY}}$** 0: Tape is writable 1: Tape is write protected (or not set)

		TEND 0: Data recorder is running 1: Data recorder is down **$\overline{\text{VBLANK}}$** 0: Vertical blanking period 1: Vertical display period VBLANK is a signal from the graphics controller
	W	Cassette control Bit: 7 6 Five Four 3 2 1 0 signal: MIC $\overline{\text{REC1}}$ **MIC** Audio track recording source — 0: Line input 1: Microphone input **$\overline{\text{REC1}}$** Play / record audio track — 0: Recording 1: Playback
E2h	W	8255 Port C Bit: 7 6 Five Four 3 2 1 0 signal: WRITE $\overline{\text{REC2}}$ KINH $\overline{\text{OPEN}}$ BST SOUND NST VGATE * Only the functions of MZ-2500 / 2000 mode are described. **WRITE** Data written to the data recorder **$\overline{\text{REC2}}$** Data track playback / recording — 0: Recording 1: Playback **KINH** REW / FF / STOP button enabled / disabled — 0: Enabled 1: Disabled **$\overline{\text{OPEN}}$** Eject with 1 → 0 → 1 **BST** Start boot state **SOUND** BEEP output **NST** Start normal state **VGATE** Screen display — 0: Display output 1: No display output VGATE forces the screen display to be solid black
E3h	W	8255 control • Bitset / reset Bit: 7 6 Five Four 3 2 1 0 signal: 0 — Bit number of port C — 0: Reset 1: Set • Mode set * Set to 82h for MZ-2500 Bit: 7 6 Five Four 3 2 1 0 signal: 1 ModeA PortA PortCH ModeB PortB PortCL **ModeA** Port A operating mode — 1x: Mode 2 01: Mode 1 00: Mode 0 **ModeB** Port B operating mode — 1: Mode 1 0: Mode 0 **PortA** Port A input / output — 0: Output 1: Input **PortB** Port B input / output — 0: Output 1: Input **PortCH** Port C upper nibble input / output — 0: Output 1: Input

		PortCL	Port C lower nibble I / O	0: Output 1: Input

8253 PIT

CLK0: 31.25kHz
CLK1: OUT0
CLK2: OUT1
It is possible to interrupt at the rising edge of OUT0.

address	R / W	Explanation
E4h	R / W	8253 Ch.0 Counter read / write
E5h	R / W	8253 Ch.1 Counter Read / Write
E6h	R / W	8253 Ch.2 Counter read / write
E7h	W	8253 Control **Bit** 7 6 Five Four 3 2 1 0 **signal** SC1 SC0 RL1 RL0 M2 M1 M0 BCD **SC1, SC0** Counter selection: 00: Ch.0 / 01: Ch.1 / 10: Ch.2 / 11: Invalid **RL1, RL0** Read / Load: 00: Counter latch operation / 01: Access the lower byte of the counter 10: Access the upper byte of the counter 11: Access the lower byte of the counter → the upper byte consecutively **M2, M1, M0** Mode selection: 000: Mode 0 (Interrupt on Terminal Count) / 001: Mode 1 (Programmable One-Shot) / x10: Mode 2 (Rate Generator) / x11: Mode 3 (Square Wave Generator) / 100: Mode 4 (Software Triggered Strobe) / 101: Mode 5 (Hardware Triggered Strobe) **BCD** Count mode: 0: 16 Bit Binary / 1: 4 Digit BCD

address	R / W	Explanation
F0h : F3h	W	8253 GATE0, GATE1 When outputting to this port, a Low pulse is output to GATE0, GATE1.

Z80B PIO (keyboard)

1 weight is added at the time of access

address	R / W	Explanation
E8h	W	Z80PIO port A data **Bit** 7 6 Five Four 3 2 1 0 **signal** DISP HCLG CH80 STB [4] STB [3: 0]

		STB [3: 0]	Key strobe output	
		STB [4]	Key strobe control	0: Read the result of ANDing all the columns of the key matrix 1: Read the columns of the key matrix specified by STB [3: 0]
		CH80	Text screen digits	0: 40-digit horizontal mode 1: 80-digit horizontal mode
		HCLG	MZ-2000 / 80B mode VRAM switching	0: Graphic 1: Text
		DISP	MZ-2000 / 80B mode VRAM switching	0: Main RAM 1: VRAM
E9h	W	Z80PIO port A control		
EAh	R	Z80PIO port B data **Bit** 7 6 Five Four 3 2 1 0 **signal** Key data		
EBh	W	Z80PIO port B control		

Key matrix

\ Strobe Data \	0	1	2	3	Four	Five	6	7	8	9	Ten	11	12	13
D7	F8	---	7	BREAK	G	O	W	,	7		/			
D6	F7	+	6	→	F	N	V	..	6	[	*			
D5	F6	..	Five	←	E	M	U	_	Five	@	Esc			
D4	F5	,	Four	↓	D	L	T	¥	Four	---	BS	CTRL		
D3	F4	9	3	↑	C	K	S	^ ^	3	;	INST DEL	Kana		
D2	F3	8	2	CR	B	J	R	Z	2	::	CLR HOME	SHIFT		
D1	F2	F10	1	SPACE	A	I	Q	Y	1	9	COPY	LOCK	conversion	HELP
D0	F1	F9	0	TAB	/	H	P	X	0	8	]	GRAPH	No conversion	

Rows 1, 2 and 10 are numeric keys When STB Bit4 = 0, the ANDed version of all Rows can be read as key data (keyboard collection / PFU)

CRT controller

address	R / W	Explanation
F4h	W	There is no auto-increment function to select the register to be written with F5h
	R	Blanking signal on the text screen

		Bit 7 6 Five Four 3 2 1 0 **signal** HB VB **HB** Horizontal blanking signal: 0: Horizontal blanking period 1: Horizontal display period **VB** Vertical blanking signal: 0: Vertical blanking period 1: Vertical display period
F5h	W	Write port to the CRT controller register specified by F4h
F6h	W	**Bit** 7 6 Five Four 3 2 1 0 **signal** MG GE RE BE **MG** 0: Overlay graphics on monochrome display 1: Do not overlay graphics on monochrome display **GE** 0: Do not output graphic Green 1: Output graphic Green **RE** 0: Do not output graphic Red 1: Output graphic Red **BE** 0: Do not output graphic Blue (do not output I plane in 16 color mode) 1: Output graphic Blue (also output I plane in 16 color mode) GE, RE, BE behave differently in 16-color mode and 256-color mode IGRB applied to each bit after passing through the palette register in 16-color mode Final output in 256-color mode (after switching the I signal) , 256 out of 512 colors) MG applied to each RGB component affects only monochrome digital output
F7h	W	**Bit** 7 6 Five Four 3 2 1 0 **signal** C **C** 0: 16 line mode 1: 8 line mode

CRT controller internal register

register	Explanation
00h	**Bit** 7 6 Five Four 3 2 1 0 **signal** K CP WM G16 **K** Number of lines to display: 0: Vertical 25-line mode 1: Vertical 20-line mode **CP** Text screen function selection: 00: Text 64 color display mode 01: Output only the first side (select this for 80 digits) 10: Output only the second side 11: Superimpose the first side and the second side The first side has high priority **WM** Overlay mode: 0: Display the graphic screen in the transparent part of the text screen 1: Display the background color in the transparent part of the text screen (display the graphic screen only in the part where the priority of the graphic is high) **G16** 8 colors / 64 colors selected: 0: Graphic 256 color / text 64 color mode 1: Graphic 16 color / text 8 color mode
01h, 02h	Display start address **Port** 02h 01h **Bit** 7 6 Five Four 3 2 1 0 7 6 Five Four 3 2 1 0 **signal** SA

03h

Text screen vertical display start line

Bit	7	6	Five	Four	3	2	1	0
signal	SL							

Standard value	SL
At 200 rasters	38 (26h)
At 400 rasters	17 (11h)

05h

Text screen vertical blank start line

Bit	7	6	Five	Four	3	2	1	0
signal	EL							

Standard value	EL
At 200 rasters	238 (FEh)
At 400 rasters	217 (D9h)

07h

Text screen horizontal display start digit

Bit	7	6	Five	Four	3	2	1	0
signal		SC						

Standard value		SC
80 digits	200 raster	11 (0Bh)
	400 raster	9 (09h)
40 digits	200 raster	10 (0Ah)
	400 raster	8 (08h)

08h

Text screen horizontal blank start digit

Bit	7	6	Five	Four	3	2	1	0
signal		EC						

Standard value		EC
80 digits	200 raster	91 (5Bh)
	400 raster	89 (59h)
40 digits	200 raster	90 (5Ah)
	400 raster	88 (58h)

09h

Display start line

Bit	7	6	Five	Four	3	2	1	0
signal					VD			

Setting range is 0 to 7 in 25-line mode and 0 to 9 in 20-line mode.

0Ah

Graphic 256-color mode I signal switching

Bit	7	6	Five	Four	3	2	1	0
signal			GIC		RIC		BIC	

xIC	I signal switching	00: I0 01: I1 10: 1 (fixed value) 11: 0 (fixed value)

In the graphic screen 256 color mode,
the values of R0 / B0 / G0 plane are used for bit 2 and the value of R1 / B1 / G1 plane is used for bit 1 and bit 0 is set to this register. Select with

0Bh, 0Ch

Background color

Port	0Ch								0Bh							
Bit	7	6	Five	Four	3	2	1	0	7	6	Five	Four	3	2	1	0

signal		G	R	B

In 16-color mode, the most significant bit (0Ch Bit0, 0Bh Bit5, 0Bh, Bit2) of each GRB is used as GRB, and in
16-color mode , 0Bh Bit0 is used as I. In 16-color mode, the color code (after applying the palette) of the graphic screen. 0 part is displayed in background color In
256 color mode, the part where the color code of the graphic screen MSB plane (after applying the palette) is 0 and the color code of LSB plane is 0 is displayed in background color To be done

0Fh

Bit	7	6	Five	Four	3	2	1	0
signal					200	1	MOD	

200	Number of display lines (screen output timing switching)	0: High resolution mode (24kHz), 400 rasters 1: Standard resolution mode (15kHz), 200 rasters	Set to match the state of the CRT switch Normally IPL is set, so there is no need to set it.
MOD	Compatibility mode	00: MZ-2500 mode (usually specified) 01: Change to MZ-2000 mode 10: Change to MZ-80B mode 11: Fixed to MZ-2500 mode	

80h : 8Fh

Graphic palette (16)

Bit	7	6	Five	Four	3	2	1	0
signal				PRx	CCx			

PRx	Display priority	0: The color of this palette number has a lower priority than the text screen 1: The color of this palette number has a higher priority than the text screen
CCx	Color code (IGRB)	

In 256-color mode, the graphic palette is applied only to the first side of the graphic screen. When two screens in 16-color mode are overlaid, the palette is applied to both the first and second sides.

Joystick

EFh

R

Joystick state

Bit	7	6	Five	Four	3	2	1	0
signal			$\overline{\text{TRGB}}$	$\overline{\text{TRGA}}$	$\overline{\text{RIGHT}}$	$\overline{\text{LEFT}}$	$\overline{\text{BACK}}$	$\overline{\text{FWD}}$

W

Joystick control

Bit	7	6	Five	Four	3	2	1	0
signal		SEL	COM2	COM1	TRGB2O	TRGA2O	TRGB1O	TRGA1O

TRGA1O	Port 1 trigger A output	0: Output L to trigger A on port 1 1: Trigger A on port 1 is input (output H)
TRGB1O	Port 1 trigger B output	0: L is output to trigger B of port 1: Trigger B of port 1 is input (outputs H)
TRGA2O	Port 2 trigger A output	0: L is output to trigger A of port 2 1: Trigger A of port 2 is input (outputs H)
TRGB2O	Port 2 trigger B output	0: L is output to trigger B of port 2 1: Trigger B of port 2 is input (H is output)
COM1	Port 1 common output	0: Output L 1: Output H
COM2	Port 2 common output	0: Output L 1: Output H
SEL	Select port to read	0: Port 1 1: Port 2

If you just want to read the joystick normally, you can write 0Fh (port 1) or 4Fh (port 2).

Printer

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>FEh</td><td>R / W</td><td>Printer control
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>R / W</th><td colspan="2">W</td><td></td><td colspan="4">R</td></tr>
<tr><th>signal</th><td>$\overline{\text{STB}}$</td><td>$\overline{\text{PRIM}}$</td><td></td><td>1</td><td>1</td><td>$\overline{\text{STA}}$</td><td>BUSY</td></tr>
</table></td></tr>
<tr><td>FFh</td><td>W</td><td>Printer data output
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>signal</th><td colspan="8">Data</td></tr>
</table></td></tr>
</table>

4096 color palette board

16-bit I / O access required

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>AEh</td><td>W</td><td>4096 color palette

Address [15: 8]
<table>
<tr><th>Bit</th><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>Ten</td><td>9</td><td>8</td></tr>
<tr><th>signal</th><td colspan="3"></td><td colspan="3">PALNO</td><td colspan="2">G / $\overline{\text{RB}}$</td></tr>
</table>
<table>
<tr><th>G / $\overline{\text{RB}}$</th><td>0: Write DATA [3: 0] to the blue component of palette number PALNO ・ Write DATA [7: 4] to the red component
1: Write DATA [3: 0] to the green component of palette number PALNO</td></tr>
</table></td></tr>
</table>

Enable / disable of the pallet board is controlled by IOA [2] of OPN.
Palette number 0 is fixed to black (RGB = 000). Writing is invalid

MZ-1R37 640K EMM

16-bit I / O access required

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>ACh</td><td>W</td><td>Address Latch Write
EMM Address [19:16] = {A15-A8}, EMM Address [15: 8] = {D7-D0}</td></tr>
<tr><td rowspan="2">ADh</td><td>R</td><td>Data read
EMM address [7: 0] = {A15-A8}, data = {D7-D0}</td></tr>
<tr><td>W</td><td>Data write
EMM address [7: 0] = {A15-A8}, data = {D7-D0}</td></tr>
</table>

* There is no auto-increment of the address.
  1 wait is added for reading and writing data.

MZ-1E30 SASI I / F

<table>
<tr><th>address</th><th>R / W</th><th>Explanation</th></tr>
<tr><td>A4h</td><td>R / W</td><td>SASI Data</td></tr>
<tr><td>A5h</td><td>W</td><td>SASI Selection
<table>
<tr><th>Bit</th><td>7</td><td>6</td><td>Five</td><td>Four</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>signal</th><td></td><td>SEL</td><td></td><td>RST</td><td></td><td colspan="3"></td></tr>
</table></td></tr>
</table>

	R	SASI Status **Bit** 7 6 Five Four 3 2 1 0 **signal** REQ ACK BSY MSG C / D I / O
A8h	W	BIOS ROM address Latch write ROM address [19:16] = {A15-A8}, ROM address [15: 8] = {D7-D0}
A9h	R	BIOS ROM data read ROM address [7: 0] = {A15-A8}, data = {D7-D0}

* There is no automatic address increment

MZ-1E35 ADPCM board (Y8950)

ϕM =
Add 1 weight when accessing 3.58MHz ?

address	R / W	Explanation
98h	W	Register number
	R	status
99h	R / W	Register access

The following functions are assigned to GPIO of Y8950 (bit assignment unknown)

- Line input ON / OFF
- Microphone input ON / OFF
- Output level (x1 / x0.5)
- Line output ON / OFF

TV control (MZ-2531 only)

address	R / W	Explanation
AFh	R	TV POWER input signal **Bit** 7 6 Five Four 3 2 1 0 **signal** TVPOWER
	W	TV CONTROL output signal **Bit** 7 6 Five Four 3 2 1 0 **signal** TVCTRL

Return